17.2 A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS

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For extremely-scaled CMOS technologies, supply voltages well below 1V will be required to maintain reliability [1]. Analog and RF design with standard devices then becomes very challenging because of the significant reduction in both the available signal swing and the available overdrive for biasing. We present ultra-low-voltage design techniques that maintain all node voltages between the supply rails, and demonstrate them in the fractional-N RF synthesizer shown in Fig. 17.2.1, which was realized in 90nm CMOS. The VCO, phase-frequency detector (PFD) and charge pump (CP) nominally operate from a 0.5V supply while the divider uses a 0.65V supply.

The VCO topology in Fig. 17.2.2 was selected and appropriately sized to maintain the common-mode output voltage close to $V_{DD}/2$, so that the output signal swings within the supply rails. For continuous tuning, varactors compatible with this VCO biasing are implemented with PMOS transistors with their sources and drains shorted and connected to the 0.2 to 0.5V tuning voltage; over this tuning range the transistors operate from depletion towards inversion. For discrete frequency tuning, the use of MIM capacitors with series switches requires very large switch sizes to limit resistive switch ON losses due to the limited 0.5V switch control levels; the associated large capacitive parasitics in the switch OFF state would lead to a limited tuning range. Discretely switching PMOS varactors with a 0 to 0.5V control signal allows us to implement a fine discrete programming step. The switched varactors are laid out with unit cells that are switched using a thermometer code to guarantee a monotonically switched tuning characteristic. The VCO nominally operates at 2.5GHz with a 4mA current bias from a 0.5V supply. The center-tapped octagonal tank inductor is constructed with metal layers 8 and 9 in parallel and has a simulated Q of 9 at 2.5GHz, while the simulated varactor Q is about 30 at 2.5GHz. The measured tuning curves in Fig. 17.2.7 show that the VCO can be tuned from 2.4 to 2.6GHz with 16 capacitor settings and the continuous tuning ranges vary from 25 to 60MHz for different capacitor settings.

The programmable divider shown in Fig. 17.2.4 adopts a truly modular architecture using a cascade of divide-by-2/3 stages, which simplifies the control word generation. The first four high-frequency divide-by-2/3 sections of the divider use composite current-mode logic latches, which combine the logic and latch functions in one circuit. The length of the stacked transistors is increased to twice the minimum length to take advantage of the V_{th} reduction caused by the reverse short-channel effect. The stacked transistors are further placed in a deep N-well and forward-body biasing [2] is used to reduce their V_{th} and enhance their transconductance. In the first divider stage, the cross-coupled latch transistor pairs are sized smaller than the logic transistors and the divider's clock port is DC biased to set its self-oscillation frequency between 2 and 3GHz, which maximizes the divider sensitivity over the VCO operating range. Among the different divider topologies studied, this divider topology resulted in the smallest gate delay and highest operating speed for ultra-low voltage operation; in simulation, it operated correctly over process, voltage and temperature (PVT) corners with a nominal supply of 0.5V. The last 7 divide-by-2/3 sections have been implemented with standard library logic cells. Modulus extension logic is included for the last stages to increase programming flexibility. In simulation, the standard logic library cells can operate up to 200MHz over PVT corners with a nominal supply down to 0.5V.

The reference buffer takes the 16MHz reference clock from an external crystal oscillator and clocks the phase-frequency detector. The 24b delta-sigma modulator (DSM) uses a MASH-111 topology to guarantee the full fractional modulus range. The register length is truncated after the first modulator stage to reduce the number of registers and the associated switching noise. The DSM uses the opposite clock triggering polarity than the phase detector logic to avoid crosstalk. The three delta-sigma stages are further clocked with offset clocks to avoid simultaneous switching. The DSM toggles the divider modulus (N) starting from the control bit of the third stage on, to prevent switching noise being injected into the VCO through the substrate; the first and second divider stages would introduce more background noise if switched by the DSM. The output pattern of a MASH 111 modulator ranges from –3 to +4 so that the modulus is toggled between N–12 to N+16 with a step size of 4. The extra quantization phase-noise resulting from the shifting is suppressed by appropriate loop filter design. The digital blocks were also realized using standard library logic cells, which operate down to 0.5V in simulation.

The use of a passive loop filter avoids the excess noise associated with active loop filters. The ultra-low supply voltage limits the headroom for the charge pump and, therefore, a source-switched topology is adopted and cascode transistors have been eliminated. The charge pump current can be digitally controlled to change the PLL bandwidth since a fixed external loop filter was used in this prototype. The charge pump output voltage varies between about 0.2 and 0.45V over the synthesizable frequency range. In packet-based communication applications where the PLL frequently turns ON and OFF, the fine discrete frequency tuning resolution provided in the VCO can be exploited to center the VCO tuning voltage close to $2/3V_{DD}$ for optimal charge pump performance.

The chip was fabricated in a digital 90nm CMOS process using only regular V_{th} devices. The die micrograph is shown in Fig. 17.2.5. In the fabricated prototype, the high-resistivity poly resistors are at 50% of their nominal value, which is outside the ±30% resistor process corners used during design and simulation. During testing, the divider power supply, DV_{DD}, which is shared with most of the digital control circuits, had to be raised to 0.65V in order to compensate for the resistance variation; the remainder of the chip was not affected and was operated from a nominal supply of 0.5V. Figure 17.2.6 shows the measured phase-noise output spectrum of the PLL for a fractional division of 162.7131 with an output frequency of 2.603097GHz. Figure 17.2.3 summarizes the measured nominal performance of the synthesizer; the power consumption is 2mW for the VCO, 4mW for the synthesizer loop, and 3mW for the 0.5V differential 50-ohm load driver, which outputs -8.5dBm. The performance is compatible with 2.4GHz ISM band applications such as Bluetooth [3] except for a required re-centering of the VCO tuning range.

Acknowledgments:
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References:
[1] *"The International Technology Roadmap for Semiconductors"*, http://public.itrs.net, 2005.
[2] S. Narendra et al., "Ultra-Low Voltage Circuits and Processor in 180nm to 90nm Technologies with a Swapped-Body Biasing Technique," *ISSCC Dig. Tech. Papers*, pp. 156–157 2004.
[3] D. Leenaerts et al., "A 15-mW Fully Integrated I/Q Synthesizer for Bluetooth in 0.18-um CMOS," *IEEE J. Solid-State Circuits*, pp. 1155-1162, July, 2003.

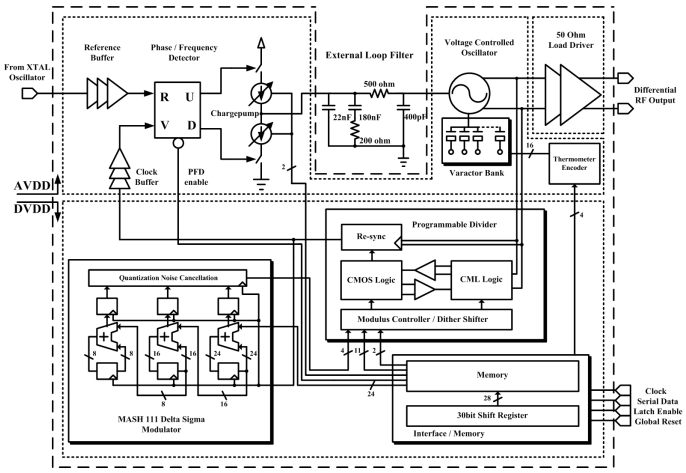

Figure 17.2.1: Block diagram of the fractional-N synthesizer.

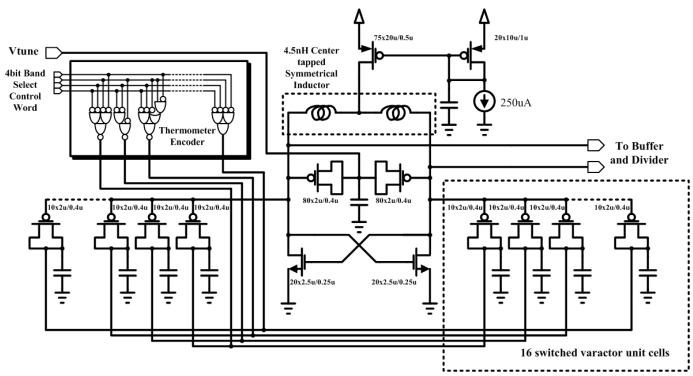

Figure 17.2.2: Schematic of the 0.5V VCO with continuous and discrete tuning.

Supply voltage [V] AVDD (VCO, PFD, CP) DVDD (Divider, DSM, interface)	0.5 0.65	
Tuning Range	225MHz	
Phase Noise (dBc/Hz):	Integer N=162	Fractional N=162.7131
@10 kHz	-68	-70
@1MHz	-113	-111
@2MHz	-120	-117
@3MHz	-123	-121
Integrated RMS Phase Error (degree) (1kHz to 100MHz)	3.9	4.4
Residual FM (kHz) (1kHz to 500kHz)	4.6	5.2
Power Consumption AVDD DVDD	 2.5mW 3.5mW	
Spurs	-52dBc@16MHz	
Chip Active Area Technology	700 um x 200um 90nm CMOS with RVT devices	

Figure 17.2.3: Measured Synthesizer Performance.

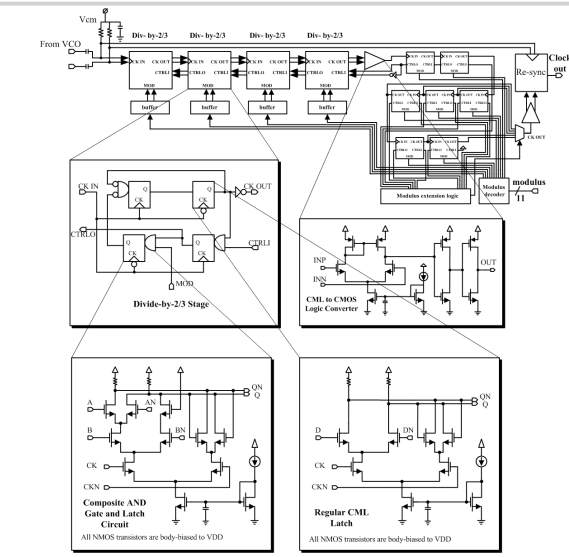

Figure 17.2.4: Architecture and circuit implementation details for the programmable divider.

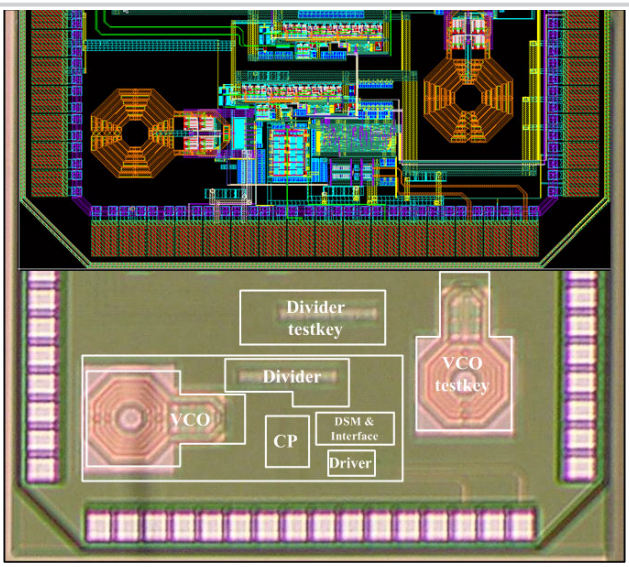

Figure 17.2.5: Die micrograph and layout composite.

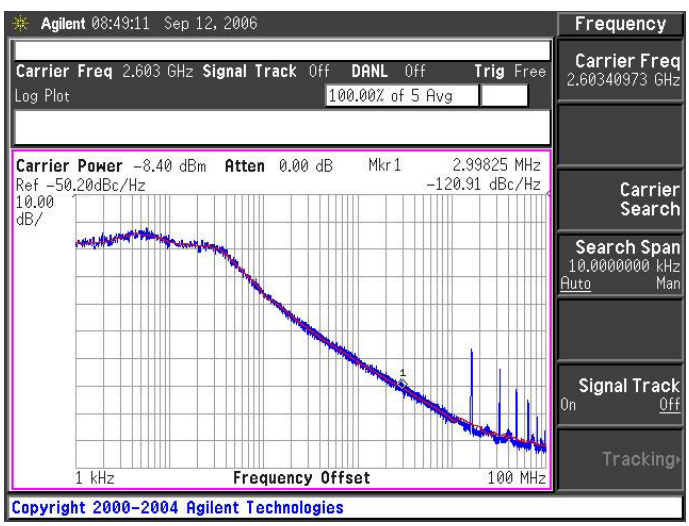

Figure 17.2.6: Measured phase-noise spectrum for a 162.7131 division ratio.

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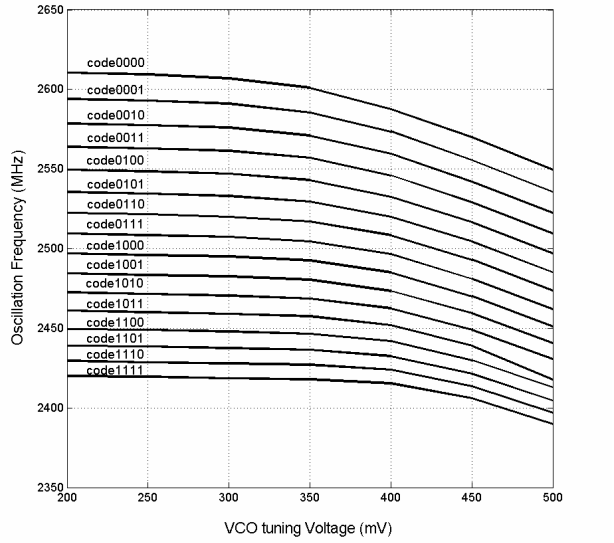

Figure 17.2.7: Measured VCO tuning curves.

